REMARKS

Claims 1-21 are pending. By this Amendment, claims 1, 6-8, 13-15, and 21 are cancelled, claims 2, 5, 9, 11, 12, 16, 17, and 20 are amended and new claims 22-24 are added.

35 USC § 112 Rejections

Claims 5, 12, and 20 stand rejected under 35 USC § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The Office Action finds the term "implicit wired operations" to be vague and indefinite and as well finds the term "function procedural operations" to be indefinite. Applicant respectfully traverses this rejection and contends that these are terms that are understood by those skilled in the art. The Examiner is referred to an On-line Verilog HDL Quick Reference Guide written by Stuart Sutherland or to http://www.sutherland-hdl.com/on-line_ref_guide/vlog_ref_top.html containing the reference guide for discussion of these terms; specifically see, implicit wired operation at pp. 5, 33; wand and wor, p. 8; function definitions p. 22. The Examiner is also referred to The Verilog Hardware Description Language, by Donald E. Thomas and Philip Moorby, which is considered the definitive text to Verilog HDL. Applicant is willing to provide the above noted resources if they are unavailable to the Examiner.

The term "implicit wired operation" is referred to within the specification at page 23, lines 8-14. As described in the patent application text, the use of the adjective "implicit" instructs someone with ordinary skill in the art of digital simulator development that the well understood AND logic gate (for wired AND operation) and OR logic gate (for wired OR operation) must be utilized. The paragraph at page 23, lines 8-14 has been amended to specifically use the term implicit wire operation so as to clarify the language of the claim.

Within the present application, the description of the preferred embodiment describes the invention by breaking Verilog down into its language constructs. "Function procedural

operation" is referred to in the prior art section 3 at page 5, line 15 through page 6, line 1 (page 6, line 1 states "Functions only contain timing free procedural constructs.") and in the Detailed Description of the Preferred Embodiments at page 28, lines 3-5. The term "function procedure operation" instructs someone of ordinary skill in the art that the "function" implementation algorithm for the PLI model compiler needs careful handling of function arguments that differ from C computer language function implementation.

Claim Interpretation

Applicant disagrees with the Examiner's interpretation of the term "implicit wire operations." The Examiner has treated the term as simply "wire operations," however, one skilled in the art would know that this interpretation is incorrect. As explained above, "implicit wire operations" is a term that is understood by those skilled, use of the adjective "implicit" instructs someone with ordinary skill in the art of digital simulator development that the well understood AND logic gate (for wired AND operation, "wand") and OR logic gate (for wired OR operation, "wor") must be utilized. The present invention's method utilizes the implicit wire operation to help achieve a simulator brand independence using the PLI. The generated C code that implements a model must evaluate wires as if there were an implicit gate inserted. Note, that in normal digital simulation technology, a wire connection involves no extra computer code execution as it does here.

Applicant also disagrees with the Examiner's interpretation of the term "timing-free procedural operations" as used in claims 5, 12, and 20. The Examiner states that it is obvious for one of ordinary skill in the art to treat "timing-free procedural operations" as part of functional procedural operations." This statement is incorrect. Timing-free procedural regions apply to any sequence of HDL code that does not have timing controls, but HDL procedures are different objects that run in zero time.

35 USC § 102 Rejections

Claims 1-21 stand rejected under 35 USC § 102(b) as being anticipated by Steinmetz, U.S. Patent No. 5,600,579. In view of the rejection, Applicant has cancelled independent claims 1, 8, and 15, and provided new claims 22-24 in place thereof. Independent claims 22-24 more clearly claim the patentable subject matter of the present invention.

Specifically, each new independent claim recites, in one form or another, that the present invention is a compiler that takes electronic circuit model portions, previously coded in at least two different HDLs, and converts the portions to simulator-independent programs; the simulator-independent programs are singularly configured (e.g., use the same object code sequence) regardless of the HDL used to code the circuit portion. Further, each independent claim recites, in one form or another, that the simulator-independent program has been enabled to make calls to a programming language interface (PLI) of a simulator regardless of the HDL of the simulator.

The above-noted features distinguish the present invention from the prior art. In rejecting all claims, the Office Action notes that "binary object code is utilizable by substantially all types of simulators." It is true that the philosophical concept "binary object code" is used by all simulators, but, as noted within Applicant's prior art discussion (see prior art section VIII, section 4, starting on page 15 of the application) different simulator brands require different sequences of "binary object code." Specifically, circuit models are currently compiled into binary instruction sequences customized for a particular brand of simulator and can only be used for that particular simulator brand. The claimed invention generates a binary instruction sequence that works with any simulator brand.

With regard to the Steinmetz patent, Applicant submits that in view of the newly submitted claims Steinmetz is no longer relevant. Steinmetz solves a problem in hardware and software co-verification. The PLI in the Steinmetz invention is used only to communicate between the master model and user written test scripts (see Cols. 19 and 20). Steinmetz discloses

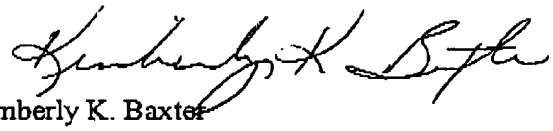
nothing related to HDL model compilers, which is now claimed by applicant by virtue of independent claims 22-24.

Because of the newly submitted independent claims, the specific 102 rejections are not addressed.

In view of the foregoing, it is submitted that this application is in condition for allowance. Favorable consideration and prompt allowance of the application are respectfully requested.

The Examiner is invited to telephone the undersigned if the Examiner believes it would be useful to advance prosecution.

Respectfully submitted,



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